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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/530,553	07/21/2000	GERALD DEBOY	POO0578	6916

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EXAMINER	
BROCK II, PAUL E	
ART UNIT	**PAPER NUMBER**
2815	

DATE MAILED: 07/21/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/530,553	DEBOY ET AL.	
	Examiner	Art Unit	
	Paul E Brock II	2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 April 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *16 and 20-56* is/are pending in the application.

4a) Of the above claim(s) *39-44 and 49-56* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *16,20-38 and 45-48* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☒ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

1. Previously submitted claims 39 – 44 and 49 – 56 are directed to an invention that is independent or distinct from the invention originally claimed for the following reasons:

Applicant elected with traverse species II, drawn to a species disclosed in figure 5b, in paper number 11. Claims 39 – 44 and 49 – 56 are drawn to non-elected species.

Since applicant has received an action on the merits for the originally presented invention, this invention has been constructively elected by original presentation for prosecution on the merits. Accordingly, claims 39 – 44 and 49 – 56 are withdrawn from consideration as being directed to a non-elected invention. See 37 CFR 1.142(b) and MPEP § 821.03.

Information Disclosure Statement

2. The listing of references in the arguments submitted April 30, 2004 is not a proper information disclosure statement. 37 CFR 1.98(b) requires a list of all patents, publications, or other information submitted for consideration by the Office, and MPEP § 609 A(1) states, "the list may not be incorporated into the specification but must be submitted in a separate paper." Therefore, unless the references have been cited by the examiner on form PTO-892, they have not been considered. The reference to Baliga has not been cited.

Drawings

3. The corrected or substitute drawings were received on December 2, 2002. These drawings are approved.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting directly or indirectly from an international application filed before November 29, 2000. Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

5. Claim 31 is rejected under 35 U.S.C. 102(e) as being anticipated by Shinohe et al. (USPAT 5969400, Shinohe).

With regard to claim 31, Shinohe discloses in figure 14 a semiconductor chip. Shinohe discloses in figure 14 a substrate having a major surface. Shinohe discloses in figure 14 a field of high voltage semiconductor components (42, 45, 53, etc.) defining a high voltage portion in

the substrate. Shinohe discloses in figure 14 an edge structure at an edge of the high voltage portion, the edge structure separating the high voltage portion of the substrate from an edge of the major surface of the substrate. Shinohe discloses in figure 14 at least one inner-zone (portion between 47 and D, not 52) of a first conductivity type (n) defining a ring structure around the field of high voltage semiconductor components at the major surface. Shinohe discloses in figure 14 at least one floating guard ring (52) of a second conductivity type (p) arranged in the at least on inner zone. Shinohe discloses in figure 14 at least one inter-ring zone (between 52's) of the first conductivity type arranged in the at least one inner zone, the at least one inter-ring zone being adjacent to the at least one floating guard ring. Since the geometry shown in figure 14 of Shinohe is the same as at least one of the geometries disclosed in the current application, it follows that Shinohe discloses in figure 14 and column 14, line 52 – column 15, line 18 at least one of the inter-ring zone and the floating guard ring being of a conductivity (n and p, respectively) and a geometry such that their free charge carriers are totally depleted when a blocking voltage is applied, the at least one inter-ring zone and the at least one floating guard ring inherently having a net doping level over a whole surface area of the major surface of the at least one inner zone.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person

having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 16, 20 – 23, 25 – 20, 32, 34 – 38, and 46 – 48 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shinohe in view of Hshieh et al. (USPAT 5930630, Hshieh).

With regard to claim 16, Shinohe discloses in figure 14 a high voltage semiconductor component. Shinohe discloses in figure 14 a semiconductor body having a high voltage region and having an edge region of the high voltage region, a high voltage resistant structure at the edge region having at least one inner zone (portion between 47 and D, not 52) of a first conductivity type adjacent to a first surface of said semiconductor body. Shinohe discloses in figure 14 a cell field (portion under 49) including high voltage components in the high voltage region. Shinohe is silent to teaching that high voltage individual components are connected in parallel. Hshieh teaches in figures 5f a cell field (portion under S) including individual high voltage components (125) in a high voltage region, the high voltage individual components being connected in parallel (S) and arranged in individual cells. It would have been obvious to one of ordinary skill in the art at the time of the present invention to use the individual high voltage components of Hshieh in the device of Shinohe in order to improve device ruggedness as stated by Hshieh in column 3, lines 58 – 64. Shinohe discloses in figure 14 at least one floating guard ring (52) of a second conductivity type arranged in said inner zone, said at least one floating guard ring surrounding the cell field. Shinohe discloses in figure 14 at least one inter-ring zone (between 52's) of said first conductivity type respectively arranged in said inner zone, said at least one inter-ring zone being arranged adjacent the at least one floating guard ring. Shinohe inherently discloses in figure 14 that the at least one floating guard ring and the at least one inter-ring zone having respective doping levels such that a net doping level over a whole surface area

of the edge region is approximately equal to zero. Since the geometry shown in figure 14 of Shinohe is the same as at least one of the geometries disclosed in the current application, it follows that Shinohe discloses in figure 14 and column 14, line 52 – column 15, line 18 the at least one floating guard ring and said at least one inter-ring zone have conductivities (p and n, respectively) and geometries set such that their free charge carriers are totally depleted when a blocking voltage is applied.

With regard to claim 20, Shinohe discloses in figure 14 wherein said at least one floating guard ring has a U-shaped cross section.

With regard to claim 21, Shinohe discloses in figure 14 at least one space charge zone stopper (51) located at an outermost edge of said edge region of said semiconductor component.

With regard to claim 22, Shinohe discloses in figure 14 wherein said space charge zone stopper comprises a heavily doped region (47) of said first conductivity type, said heavily doped region being arranged in said inner zone.

With regard to claim 23, Shinohe discloses in figure 14 wherein said space charge zone stopper comprises a damage implanted region (47) being arranged in said inner zone.

With regard to claim 25, Shinohe does not disclose a magnetoresistor. Hshieh teaches in figure 5f at least one magnetoresistor (125) located at an inner edge of an edge region of said semiconductor component. It would have been further obvious to one of ordinary skill in the art at the time of the present invention to use the magnetoresistor of Shinohe in order to improve device performance as taught by Hshieh in the paragraph linking columns 1 and 2.

With regard to claim 26, Hshieh teaches in figure 5f wherein at least one of said magnetoresistors is simultaneously a gate electrode of said semiconductor component.

With regard to claim 27, Hshieh teaches in figure 5f wherein at least an outermost of the magnetoresistors is nearly completely enclosed by a cathode metallization (170) in a direction of the first surface of the semiconductor component.

With regard to claim 28, Hshieh teaches in figure 5f wherein said cathode metallization is a metallization of a source electrode of said semiconductor component.

With regard to claim 29, Shinohe discloses in figure 14 wherein said inter-ring zones in said edge region have a cross-section tapered to said first surface.

With regard to claim 30, Hshieh teaches in figure 5f wherein the individual high voltage components are vertical power transistors.

With regard to claim 32, Shinohe discloses in figure 14 a semiconductor chip. Shinohe discloses in figure 14 a substrate having a major surface. Shinohe discloses in figure 14 a plurality of high voltage semiconductor components in the substrate. Shinohe is silent to teaching that high voltage semiconductor components are high voltage vertical MOSFET components. Hshieh teaches in figures 5f a plurality of high voltage vertical MOSFET components in the substrate. It would have been obvious to one of ordinary skill in the art at the time of the present invention to use the high voltage vertical MOSFET components of Hshieh in the device of Shinohe in order to improve device ruggedness as stated by Hshieh in column 3, lines 58 – 64. Shinohe discloses in figure 14 an edge structure at an edge of the plurality of high voltage semiconductor components to separate the high voltage semiconductor components from a remainder of the substrate. Shinohe discloses in figure 14 at least one inner zone of a first conductivity type defining a ring structure around the plurality of high voltage semiconductor components at the major surface. Shinohe discloses in figure 14 at least one floating guard ring

of a second conductivity type arranged in the at least on inner zone. Shinohe discloses in figure 14 an inter-ring zone of the first conductivity type arranged in the at least one inner zone, the inter-ring zone being allocated to the at least one floating guard ring. Since the geometry shown in figure 14 of Shinohe is the same as at least one of the geometries disclosed in the current application, it follows that Shinohe discloses in figure 14 and column 14, line 52 – column 15, line 18 at least one of the inter-ring zone and the floating guard ring being of a conductivity and a geometry such that their free charge carriers are totally depleted when a blocking voltage is applied. Shinohe inherently discloses in figure 14 that the at least one floating guard ring and the at least one inter-ring zone having respective doping levels such that a net doping level over a whole surface area of the edge region is approximately equal to zero.

With regard to claims 34 and 46, Shinohe discloses in figure 14 wherein the at least one floating guard ring is a plurality of floating guard rings. Shinohe discloses in figure 14 the at least one inter-ring zone is a plurality of inter ring zones disposed between respective ones of the plurality of floating guard rings. Shinohe discloses in figure 14 said plurality of floating guard rings being doped at the second conductivity type. As far as the examiner can ascertain, Shinohe discloses in figure 14 the plurality of inter-ring zones being heavily doped at the first conductivity type (heavily doped compared to an undoped substrate).

With regard to claims 35 and 47, Shinohe discloses in figure 14 the floating guard ring is doped at a second conductivity type and the inter ring zones are of the first conductivity type. It is obvious to consider the floating guard ring as not having a definite boundary between the dopants of the floating guard ring and the inter-ring zones. It can therefore be considered that the floating guard ring comprises at least one layer of the second conductivity type between the

highest second conductivity concentration of the floating guard ring and the highest concentration of the first conductivity type of the inter-ring zone. One of ordinary skill in the art at the time of the present invention would obviously interpret this layer doped at the second conductivity type between respective ones of the floating guard rings and the inter-ring zones because the physical geometry of any diffusion layer would have these concentration varying properties.

With regard to claims 36 and 48, similar to the analysis of claim 35, above, but now considering the respective "second" layer of claim 36 is equivalent to the "first" layer of claim 35. A first layer of a first conductivity type would be present as varying concentrations of dopants from the "boundary" between the maximum concentration of a first conductivity type in the inter-ring zones is decreased in a direction of towards the maximum concentration of the second conductivity type in the floating guard rings. Therefore, it is further obvious to consider this additional "first" layer of first conductivity type as a physical property of the device in Shinohe.

With regard to claim 37, Shinohe discloses in figure 14 wherein the at least one floating guard ring is a plurality of floating guard rings. Shinohe discloses in figure 14 the at least one inter-ring zone is a plurality of inter ring zones disposed between respective ones of the plurality of floating guard rings. Shinohe discloses in figure 14 the plurality of floating guard rings extending into the inner zone of the semiconductor body in substantially parallel columnar cross sections disposed at a regular spacing from one another. While the cross section of the floating guard rings in figure 14 of Shinohe are not exactly parallel, they do read on being substantially parallel.

With regard to claim 38, Shinohe discloses in figure 14 wherein the plurality of floating guard rings extend to mutually different depths into the semiconductor body.

8. Claim 24 is rejected under 35 U.S.C. 103(a) as being unpatentable over Shinohe and Hshieh as applied to claims 16 and 21 above, and further in view of Hsu et al. (USPAT 5521105, Hsu).

With regard to claim 24, Shinohe discloses in figure 14 wherein said space charge zone stopper comprises an electrode (51) connected to said inner zone. Hsu is silent to an electrode material. Hsu discloses that an electrode (23) can be polysilicon. It would have been obvious to use the polysilicon of Hsu in the device of Shinohe in order to use an electrode material that is well known and widely available in the art, as well as economically feasible.

9. Claim 33 is rejected under 35 U.S.C. 103(a) as being unpatentable over Shinohe and Hshieh as applied to claim 16 above, and further in view of Omura et al. (Omura et al., "A breakdown voltage simulator for semiconductor devices with depleted floating regions", NASECODE VI. Proceedings of the Sixth International Conference on the Numerical Analysis of Semiconductor Devices and Integrated Circuits, Dublin, Ireland, 11-14 July 1989, p.372-7; Omura).

Shinohe discloses in figure 14 wherein the at least one floating guard ring is a plurality of floating guard rings. Shinohe discloses in figure 14 the at least one inter-ring zone is a plurality of inter ring zones disposed between respective ones of the plurality of floating guard rings. Shinohe discloses in figure 14 the plurality of inter-ring zones being lightly doped at the first

conductivity type (N-). Shinohe discloses in figure 14 said plurality of floating guard rings being doped at the second conductivity type (P). Shinohe and Hshieh are silent to the doping level of the floating guard rings. Omura teaches in the abstract and figure 7 a plurality of floating guard rings ($P_3 - P_6$) being lightly doped at a second conductivity type. It would have been obvious to one of ordinary skill in the art at the time of the present invention to use at least the lightly doped guard rings of Omura in the device of Shinohe and Hshieh in order to reduce the adverse effects of junction curvature as stated by Omura on page 374 in the third section, first paragraph.

10. Claim 45 is rejected under 35 U.S.C. 103(a) as being unpatentable over Shinohe as applied to claim 31 above, and further in view of Omura.

Shinohe discloses in figure 14 wherein the at least one floating guard ring is a plurality of floating guard rings. Shinohe discloses in figure 14 the at least one inter-ring zone is a plurality of inter ring zones disposed between respective ones of the plurality of floating guard rings. Shinohe discloses in figure 14 the plurality of inter-ring zones being lightly doped at the first conductivity type (N-). Shinohe discloses in figure 14 said plurality of floating guard rings being doped at the second conductivity type (P). Shinohe is silent to the doping level of the floating guard rings. Omura teaches in the abstract and figure 7 a plurality of floating guard rings ($P_3 - P_6$) being lightly doped at a second conductivity type. It would have been obvious to one of ordinary skill in the art at the time of the present invention to use at least the lightly doped guard rings of Omura in the device of Shinohe in order to reduce the adverse effects of junction curvature as stated by Omura on page 374 in the third section, first paragraph.

Response to Arguments

11. Applicant's arguments filed April 30, 2004 have been fully considered but they are not persuasive.

12. With regard to applicant's arguments that the Shinohe and Hshieh do not teach "to provide that a conductivity and a geometry in the edge termination structure is provided which together result in the effect of total depletion," it should be noted that Shinohe discloses in figure 14 and column 14, line 52 – column 15, line 18. The conductivity and geometry selected in figure 14 of Shinohe clearly read on this feature. Therefore, applicant's arguments are not persuasive and the rejection is proper.

13. In response to applicant's argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies (i.e., the precise design rule) are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993). Therefore, applicants arguments are not persuasive, and the rejection is proper.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Paul E Brock II whose telephone number is (571) 272-1723. The examiner can normally be reached on 8:30 AM - 5:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on (571) 272-1664. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Paul E Brock II